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MEMORY READOUT CIRCUIT

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/1[1]

Specification

1. Title of the invention

Memory Readout Circuit

2. Claims

1. A memory readout circuit, characterized by the fact that in a memory readout circuit in which one end of a switch being constituted by a field-effect transistor (FET) is connected to a drain terminal of a memory element, the other end is connected to a source or drain terminal of a transistor for detecting a current, the other end of said transistor for detecting a current is connected a power source, an inverter having a drain voltage of the above-mentioned memory element as an input controls the gate voltage of the above-mentioned switch, and a level detecting circuit detects the voltage of the other end of the above-mentioned switch, the above-mentioned inverter consists of a PMOS transistor and a NMOS transistor in

[1] Numbers in the margin indicate pagination in the foreign text.

which the ratio of the current amplification factor is 1:400-1:25; and when the above-mentioned memory element is in an ON state, said memory element is operated in a non-saturation region, and the above-mentioned transistor for detecting a current is operated in a saturation region.

2. The memory readout circuit of Claim 1, characterized by the fact that the switch being constituted by the above-mentioned field-effect transistor (FET) has an ON-state resistance sufficiently smaller than an ON-state resistance of the transistor for detecting a current when the memory element is in an ON state.

3. Detailed explanation of the invention

(Industrial application field)

The present invention pertains to a memory readout circuit. Especially, the present invention pertains to a current detection type memory readout circuit suitable for a small-detection current and high-speed readout.

(Background of the invention)

A conventional nonvolatile memory readout circuit is shown in Figure 6.

In Figure 6, 11 is a memory element, 21 and 22 are field-effect transistors, 23 is a normal OFF type NMOS transistor, 24

is a normal ON type PMOS transistor, 25 is a PMOS transistor, 31 is a level detecting circuit, and 32 is a waveform shaping circuit.

In a closed circuit being constituted by a transistor 22 in which one ends of the transistors 23 and 24 constituting an inverter are connected to V_{CC}, the drain voltage V_D of the /2 memory element 11 changed to an OFF state is raised at high speed and operated so that a fixed value may be maintained. In the transistor 25, the current flowing in the memory element 11 is converted into a voltage, supplied to the level detecting circuit 31, and output through the level detecting circuit 31 and the waveform shaping circuit 32 (see "storage element readout system" of Japanese Kokai Patent Application No. Sho 58[1983]-208995). The transistor 22 is set so that a large current may flow in terms of operation, and when the memory element 11 is in an ON state, a large current corresponding to the ON-state resistance flows continuously. It is an ineffective current for the current flowing in the transistor 25 for detecting a current and is not preferable in terms of constitution of a low power consumption circuit.

As a circuit in which the above-mentioned drawbacks are removed, there is a "memory readout circuit" of Japanese Patent Application No. Sho 58[1983]-134427 proposed by these inventors.

Figure 1 is a constitutional diagram showing the above-mentioned memory readout circuit.

In Figure 1, 111 is a memory element, 121 is a NMOS type field-effect transistor, 123 is a NMOS transistor, 124 and 125 are PMOS transistors, 131 is a level detecting circuit, 132 is a waveform shaping circuit, C1 is a data line capacity, and C2 is a sense circuit capacity. The difference between the above-mentioned Figures 6 and 1 is that a current drivability difference of 1:3-5 is installed between a drain current (ID) of the transistor 125 for detecting a current and a drain current (ID) of the memory element 111.

When the memory element 11 is in an ON state, a low power type readout circuit can be realized. However when the memory 111 was changed from an ON-state to an OFF-state, the readout time was largely affected, and there was no restriction condition for the drain voltage of the memory element 111 for cutting off the transistor 121, that is, the logic threshold (V_{out}) of the inverter consisting of the transistors 123 and 124, the readout time was delayed by the V_{cut} value.

(Purpose of the invention)

The purpose of the present invention is to provide a memory readout circuit that solves these conventional problems and can speed up a memory readout speed at a low power consumption

without making the memory readout time unstable by a simple inexpensive method.

(Outline of the invention)

In order to achieve the above-mentioned purpose, the memory readout circuit of the present invention is characterized by the fact that in a memory readout circuit in which one end of a switch being constituted by a field-effect transistor (FET) 121 is connected to a drain terminal of a memory element 111, the other end is connected to a source or drain terminal of a transistor 125 for detecting a current, the other end of said transistor for detecting a current is connected a power source, an inverter having a drain voltage of the above-mentioned memory element 111 as an input controls the gate voltage of the above-mentioned switch, and a level detecting circuit 131 detects the voltage of the other end of the above-mentioned switch, the above-mentioned inverter consists of a PMOS transistor 124 and a NMOS transistor 123 in which the ratio of the current amplification factor is 1:400-1:25; and when the above-mentioned memory element is in an ON state, said memory element 111 is operated in a non-saturation region, and the above-mentioned transistor 125 for detecting a current is operated in a saturation region.

(Application example of the invention)

Next, an application example of the present invention is explained by the figures. Also, in an application example of the present invention, a memory readout circuit shown in the above-mentioned Figures 1 and 2 can be applied. Figure 3 is an operation time chart of Figure 1.

In Figure 1, when a memory element 111 is in an ON state, the drain voltage of the memory element 111, that is, the data line potential (V_{OL}) is determined by the ON-state resistance ratio of the memory element 111 in transistors 125 and 121. Also, in order to eliminate the voltage drop between both the source and drain terminals of said transistors and to raise the switching speed of said transistor, the ON-state resistance of the transistor 121 is set to a value sufficiently smaller than the ON-state resistance of the transistor 125. Also, in this /3 state, a transistor 123 is in an OFF state, and a transistor 124 is in an ON state. The output of a level detecting circuit 131 is "H," and the output of a waveform shaping circuit 132 is "L." If the memory element 111 is changed from this state to an OFF state, the transistor 125 raises the data line potential by charging a data line capacity C1 and a sense circuit capacitor C2.

If the data line potential reaches the logic threshold (V_{out}) of an inverter consisting of the transistors 123 and 124,

as shown in Figure 3, the transistor 123 is turned ON, the drain voltage (V_2) is lowered to "L," and the transistor 121 is in a cut-off state. For this reason, the charge to the data line capacity C1 is stopped, and the data line potential is maintained at V_D ($\fallingdotseq V_{cut}$). On the other hand, since the charge to the sense circuit capacity C2 is continued, the detection terminal potential is further raised. If the potential reaches the value of V_{D1}, the output of the level detecting circuit 131 goes to "L," and the output of the waveform shaping circuit 132 goes to "H." Also, since there is a relationship of C1 $\geq$ C2 between the data line capacity C1 and the sense circuit capacitor C2, the transistor 121 is cut off, and the charge to the sense circuit capacity C2 is rapidly carried out, so that V_{D1} is obtained in a short time. Therefore, the memory readout time is considered as the charge time to the data line capacity C1, that is, the time until the data line potential is changed from V_{OL} to V_{CUT} (ΔV of Figure 2). The logic threshold (V_{CUT}) of the inverter consisting of the transistors 123 and 124 for setting the transistor 121 to a cut-off state is expressed by the following equation, when the NMOS threshold of the transistor 123 is V_{TN}, the PMOS threshold of the transistor 124 is V_{TP}, and the gain constants (channel conductances) of the transistors 123 and 124 are respectively β_{123} and β_{124}. However, V_{TN}, V_{TP}, and V_{CUT}

are standardized values by the power supply voltage V_{CC}, and $\beta_{R1} = \beta_{124}/\beta_{123}$.

$$V_{CUT} = V_{TN} + (1 - V_{TP})\sqrt{\beta_{R1}} \,/\, 1 + \sqrt{\beta_{R1}} \ [V] \qquad (1)$$

Also, the variation portion of V_{CUT} to the variation of each of V_{TN}, V_{TP}, and β_{R1} is expressed by the following equation.

$$\Delta V_{CUT} = \pm \{1 \,/\, 1 + \sqrt{\beta_{R1}} \cdot \Delta V_{TN} + \sqrt{\beta_{R1}} \,/\, 1 + \sqrt{\beta_{R1}}\ \Delta V_{TP} + (1 - V_{TN} - V_{TP}) \,/\, (1 + \sqrt{\beta_{R1}})3 \cdot \sqrt{\beta_{R1}} \,/\, 2 \cdot \Delta\beta_{R1} \,/\, \beta_{R1}\} \ [V] \qquad (2)$$

Figure 4 shows the relationship between β_{R1} and V_{CUT} of the transistors 123 and 124. As shown in Figure 4, if β_{R1} is decreased, the logic threshold (V_{CUT}) approaches to V_{TN} and V_{TP} and is stabilized, and ΔV_{CUT} is also decreased, so that a high-speed effect is large.

However, even if β_{R1} is extremely decreased, the effect on V_{CUT} is retarded, and the inverter size is also increased, which is not preferable in terms of manufacture. Also, since V_{TN} and V_{TP} are used in a range of 0.05-0.2 V, 1/400-1/50 as shown by a slant part of Figure 4 is obtained as an optimum value range of β_{R1}.

Figure 5 shows the relationship between β_{R1} and V_{CUT} in the slant part of Figure 4.

When β_{R1} is set in the slant part of Figure 4, each variation value (ΔV_{CUT}) of ΔV_{TN}, ΔV_{TP}, β_{R1}/R1 due to manufacture parameters in terms of working becomes values shown in Figure 5,

and only the V_{CUT} value is varied by the threshold of the NMOS transistor 123.

In other words, if only the threshold V_{TN} of the NMOS transistor 123 is sufficiently controlled in the manufacture, since the value of V_{CUT} is a stable value with little variation and ΔV (= V_{CUT} - V_{OL}) can also be small, the power consumption is reduced, and the readout time is shortened.

Next, a condition which is determined by an ON-state resistance of the memory element 111 and the current detection transistor 125 and stably sets the data line potential VOL in an ON state of the memory element 111 to a low level is mentioned.

In conclusion, it is set at a point of Figure 2, that is, in a non-saturation region in the V_D-I_D characteristic of the memory element 111 and the saturation region in the V_{D1}-I_D characteristic of the transistor 125. Under such a set condition, the rise of the V_D-I_D characteristic of the memory element 111 is steep, and since ID of the transistor 125 is constant in the vicinity of a point, V_{OL} is stabilized without /4 being largely varied. The relationship with the threshold of the memory element 111 and the transistor 125 is as follows.

The saturation operation condition of the transistor 125 is $1 - V_{OL} > 1 - V_{TP}$.

$$\therefore V_{OL} < V_{TP} \qquad (3)$$

In the non-saturation region of the memory element 111,

$$1 - V_{TM} > V_{OL} \quad (4)$$

However, V_{TM} is a threshold of the memory element 111. From the above-mentioned equations (3) and (4), the operation point can be limited by the equation (3), and $V_{OL} < V_{TP}$. Also, if $\beta_{R2} = \beta_{125}/\beta_{111}$, there is the following relationship among β_{R2}, V_{TM}, and V_{TP}.

$$\beta_{R2} = 2(1 - V_{TM})V_{OL} - V_{OL}^2 \,/\, (1 - V_{TP})^2 \quad (5)$$

If $V_{OL} << 1 - V_{TM}$ is set,

$$\beta_{R2} = 2(1 - V_{TM}) \,/\, (1 - V_{TP})^2 \cdot V_{OL} < (1 - V_{TM})\, V_{TP} \,/\, (1 - V_{TP})^2 \quad (6)$$

When $V_{TM} \fallingdotseq V_{TP}$, $\beta_{R2} < V_{TP} \,/\, 1 - V_{TP}$ (7)

From the above-mentioned equation (7), β_{R2} is 1/19-1/3 in a general range of 0.05-0.25 of V_{TP}.

In other words, β_{R2} is set to 1/3 or less. Also, since β_{R2} is almost equal to the ratio (I_{125}/I_{111}) of the ON-state current (I_{111}) of the memory element 111 and the ON-state current (I_{125}) of the transistor 125 in the saturation region of Figure 2, low power consumption, stabilization of V_{OL}, etc., are obtained, even if the ON-state current (I_{125}) of the transistor 125 is designed at 1/3 or less of the ON-state current (I_{111}) of the memory element 111.

Thus, the gate voltage V_2 of the transistor 121 for blocking the data line of the memory readout circuit shown in Figure 1 is controlled, and for the inverter consisting of the transistors 123 and 124, the gain constant of the transistors 123 and 124 is set to the relationship of $\beta_{124} / \beta_{123} = 1/400\text{-}1/25$ ($= \beta_{R1}$). On the other hand, for the transistor 125 and the memory element 111 for determining V_{OL} being an input voltage of the above-mentioned inverter, when the memory element 11 is in an ON state, the transistor 125 is operated in the saturation region, and the memory element 111 is operated in the non-saturation region. At that time, V_{OL} is set to the threshold V_{TN} or less of the NMOS transistor 123. In accordance with the above-mentioned two setup conditions, V_{CUT} is made to approach to V_{TN} and V_{TP} and is stabilized with V_{OL}, and the variation of V_{CUT} and V_{OL} can be decreased. Thus, when the capacity charge time of $(V_{CUT} - V_{OL})$ $(C1 + C2)/I'_{125}$, that is, when the memory element 11 is changed to an OFF state, the memory readout time is short and stable. Also, since the current flowing in an ON state of the memory element 111 is limited by the transistor 125, the power consumption can be reduced. Also, the above-mentioned I'125 is a charge current from the transistor 125. Also, since the ON-state current of the memory element 111 is 3-5 times of the

transistor 125, the readout time of the memory element 111 in an ON state is faster than the readout time in an OFF state.

(Effects of the invention)

As explained above, according to the present invention, as an ON/OFF state change of the memory element 111, the gain constant ratio of the transistors 123 and 124 is set to 1:400-1:25. In an ON state of the memory element 111, the memory element 111 is operated in a non-saturation region, and the transistor 125 is operated in a saturation region. Thus, without making the memory readout time unstable, the power consumption of the circuit can be lowered, and the memory readout time can be stably sped up.

4. Brief description of the figures

Figure 1 is a memory readout circuit diagram to which the present invention is applied. Figure 2 is a V_D-V_D characteristic diagram showing the transistor 125 and the memory element 111 shown in Figure 1. Figure 3 is an operation time chart of Figure 1. Figure 4 is a V_{CUT}-β_{R1} characteristic diagram of the transistors 123 and 124 shown in Figure 1. Figure 5 is a ΔV_{CUT}-β_{R1} characteristic diagram in a slant part of Figure 4. Figure 6 is a conventional memory readout circuit diagram.

11, 111 Memory elements

21, 22 FET transistors

23, 121, 123 NMOS transistors

24, 25, 124, 125 PMOS transistors

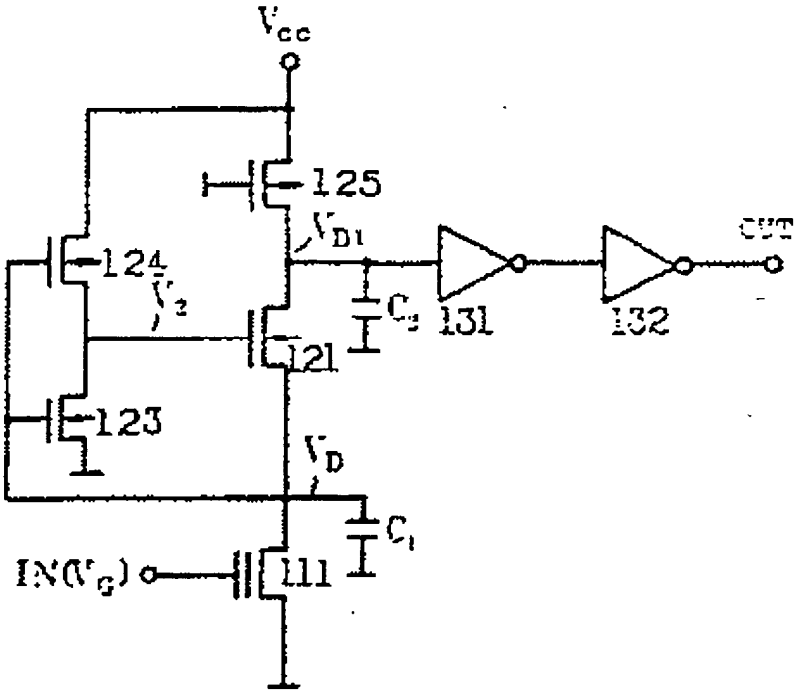
31, 131 Level detecting circuits

32, 132 Waveform shaping circuits

C1 Data line capacity

C2 Sense circuit capacity

第　1　図


Vcc
125
VD1
OUT
124
V2
C2
131
132
121
123
VD
C1
IN(VG)
111

第　2　図

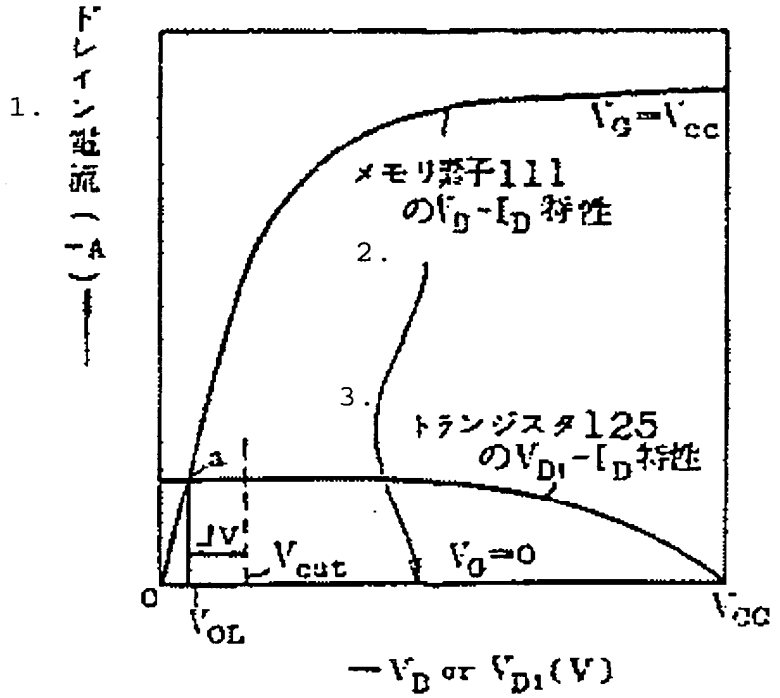

ドレイン電流 —A (—)
VG=Vcc
メモリ素子111
のVD-ID特性
2.
3.
トランジスタ125
のVD1-ID特性
a
ΔV
Vcut
VG=0
0
VOL
Vcc
—VD or VD1(V)

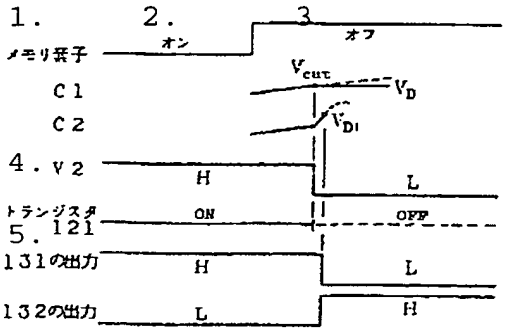
Figure 2:

1. Drain current

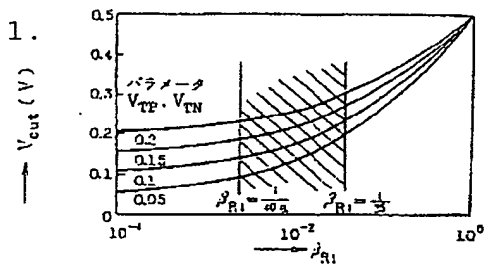
2. V_D-I_D characteristic of memory element 111

3. V_{D1}-I_D characteristic of transistor 125

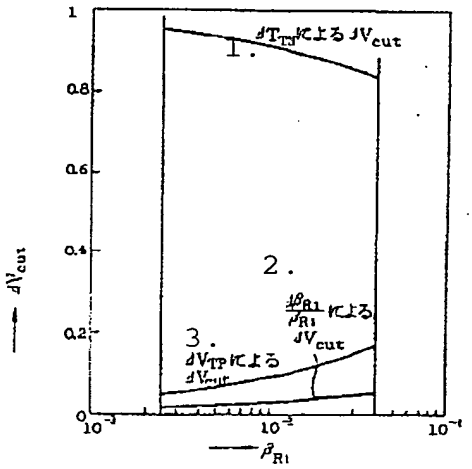
第 3 図



第 4 図



第 5 図



第 6 図

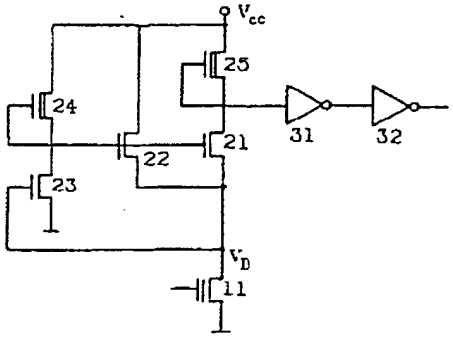


Figure 3:

1. Memory element
2. ON
3. OFF
4. Transistor 121
5. Output of 131
6. Output of 132

Figure 4:

1. Parameter

Figure 5:

1. ΔV_{CUT} due to ΔT_{TN}
2. ΔV_{CUT} due to $\Delta \beta_{R1}/\beta_{R1}$
3. ΔV_{CUT} due to ΔV_{TP}